REMARKS

Claims 1-10 are now pending in the Current Application. In an office action dated October 17, 2002 ("Office Action"), the Examiner objected to the previously submitted drawing-correction proposal because it is not in the form of a pen-and-ink sketch, referring to MPEP § 608.02(v), rejected claims 6 and 8 under 35 USC §102(b) as being anticipated by "The Harp Reconfigurable Computing System," Page, Ian, Oxford University Hardware Compilation Group, October 1994 ("Page"), rejected claims 1, 2, 4, 5, 9, and 10 under 35 USC § 103(a) as being unpatentable over Page in view of Que's Computer Users Dictionary, Fifth Edition., Pfaffenberger, Brian, 1994 ("Que"), rejected claim 3 under 35 USC § 103(a) as being unpatentable over Page in view of Que and further in view of Sudo, U.S. Patent No. 6,047,198 ("Sudo"), and rejected claim 7 under 35 USC § 103(a) as being unpatentable over Page in view of Sudo.

Applicants' representative does not understand the Examiner's objections to the previously submitted drawing-correction proposal. MPEP § 608.02(v) states that "[w]hen changes are to be made in the drawing itself, *other than mere changes in reference characters*, designations of figures, or inking over lines pale and rough, a print or pen-and-ink sketch must be filed ..." The drawing corrections amount to simply correcting two reference numerals. Applicants' representative's reading of MPEP § 608.02(v) would suggest that pen-and-ink sketches are not necessary, in this case. We have again included the proposed drawing changes, as a separate attachment to this Office-Action Response.

Applicants' representative would like to thank Examiner Meonske for discussing the Current Application in a telephone interview on Dec. 18, 2002. In that interview, the meaning and limitation potential of language included in the preamble of a claim were discussed. Applicants' representative believes that Examiner Meonske acknowledged that a preamble can include limiting language, but is unclear if the arguments currently made in the context of the Current Application by the Examiner and by Applicants' representative were resolved. The Page reference was discussed, and Applicants' representative pointed out reasons why the current claims do not read on Page. Examiner Meonske indicated that she does not have the ability to negotiate the USPTO's position with regard to the rejections, but noted the arguments presented by Applicants' representative.

Applicants' representative agreed to submit the current Office-Action Response to summarize those arguments, and to perhaps again discuss the Current Application in four to six weeks, after Examiner Meonske has had an opportunity to consider the arguments.

The 35 USC §102(B) Rejection of Claim 6 and the 35 USC § 103(A) Of Claim 1 Are Improper, Purely on the Basis of Elementary Claim Construction.

The Examiner states, in section 20 of the Office Action, in response to Applicants' representative's argument that Page's device is not a subsystem controller, states that " [h]owever, as described above in the rejections, the microprocessor, the dynamic RAM, static RAM, frequency synthesizer, and parallel expansion port work together to control the Xilinx 3195 Field Programmable Gate Array, or subsystem. Therefore, Page's device is a subsystem controller." The statement makes no sense. In the rejection of claim 6, the Examiner states that "programming logic circuits into a complex programmable logic device included in the single-IC subsystem controller (Page page 1, bullet "Xilinx 3195 Field Programmable Gate Array" constitutes the claimed element of programming control functionality into the single-IC subsystem controller, but later states, in part "c" of the claim-6 rejection, that interconnecting the Xilinx 3195 Field Programmable Gate Array to the frequency synthesizer, which generates a clock signal for the FPGA, constitutes interconnection the single I-C subsystem controller to the subsystem. Thus, in the rejection of claim 6, the Examiner has identified the Xilinx 3195 Field Programmable Gate Array as a component of a supposed subsystem controller as well as the subsystem that the subsystem controller controls. The Examiner again identifies the Xilinx 3195 Field Programmable Gate Array as a component of a supposed subsystem controller in part "a" of the rejection of claim 1, in section 9 of the Office Action, but subsequently maintains that the subsystem controlled by the subsystem controller is the Xilinx 3195 Field Programmable Gate Array, in part "f" of subsection 9. In other words, in the rejections of both claim 1 and claim 6, the Examiner's supposed subsystem controller controls itself. By elementary claim construction, the element "electronic interface to *a* device or subsystem controlled by *the* subsystem controller" clearly and unambiguously claims a device or subsystem, controlled by the subsystem controller, that is separate and distinct from the subsystem controller. Otherwise, the claimed "device or

subsystem" would need to be preceded with the article "the." The Examiner cannot use the Xilinx 3195 Field Programmable Gate Array as both the complex programmable logic device component of the subsystem controller as well as the device or subsystem controlled by the subsystem controller. For this reason alone, the 35 USC §102(b) rejection of claim 6 and the 35 USC § 103(a) of claim 1 are improper, purely on the basis of elementary claim construction.

Of course, in the context of the Specification of the Current Application, including the definition of subsystem controller, provided below, there is simply no basis for either the 35 USC §102(b) rejection of claim 6 and the 35 USC § 103(a) of claim 1:

> Subsystem controllers are ubiquitous components of modern computer systems, peripheral devices within computer systems, and other electronic devices. The term "subsystem controller" generally refers to a subcomponent of a more complex electronic system, such as a computer, that comprises logic circuits, a programmable logic device, and a general-purpose micro-controller that executes a number of software routines. A subsystem controller is generally dedicated to one or a small number of specific control tasks. For example, the control of LED and LCD display devices incorporated in a front panel display of a computer system is generally carried out by one or more subsystem controllers. Use of subsystem controllers may offload computationally intensive and time-intensive tasks from the main processor or processors of computer systems, and may significantly decrease data traffic on critical busses of the computer system that are bottlenecks for data movement within the computer system.

A subsystem controller, as defined above, needs to contain both processor and programmable logic components, and is dedicated to one or a small number of specific control tasks. The Current Application mentions LED and LCD display controllers, but many other types of subsystem controllers may be used in computer systems, including floppy-disk drive controllers and subsystem controllers that power-on and power-off cooling fans during operation of a computer system. The device of subsystem controlled by a subsystem controller is external and separate from the subsystem controller, which is why the subsystem controller requires "an additional electronic interface to a device or subsystem controlled by the subsystem controller" as claimed in claim 1. Every example disclosed in the Specification adheres to this very basic principle. The meaning of claim 1 is completely and unambiguously clear both by elementary claim construction principles as well as by the meaning of the term "subsystem controller," as defined in the Specification, and as well known to anyone with ordinary skill and knowledge of computer-system design.

The FPGA in Page's device is not a controller in any sense of the word, nor is it controlled by another component. As clearly stated by Page, "[i]n our HARP system, the FPGA subsystem is perhaps best regarded as a flexible co-processor. Once the microprocessor has loaded a configuration into the FPGA, they become equal partners in computation" (Page, last paragraph of page 3). To identify the FPGA as a subsystem controlled by some other collection of components is directly contradictory to Page's explicitly stated role for the FPGA in Page's board-level system. Please note yet another discrepancy in Page's description of the role of the FPGA in his board-level device, and that inherently attributed to the device in the Examiner's rejections. In the above-quoted definition of a subsystem controller, included in the Specification, it is clearly stated that subsystem controllers may be used to "offload computationally intensive and time-intensive tasks from the main processor or processors of computer systems, and may significantly decrease data traffic on critical busses of the computer system that are bottlenecks for data movement within the computer system." However, note that, in Page's device, where "the FPGA becomes a true co-processor," the FPGA "has its own local memory and also has full access to the bus for high-speed communications to the microprocessor" (Page, first paragraph of page 2). Page later notes that, as a true co-processor, the FPGA may be configured to run a fast "inner loop" in a computation. In essence, the FPGA used as a co-processor will not significantly decrease data traffic on critical busses, but will, instead, increase data traffic on critical busses. It is well understood, in computing, that distribution of processing tasks among discrete processing components is necessarily accompanied by increased communications costs.

<u>The Single-Integrated-Circuit Language in Both Claim 1 and Claim 6 is an Intentionally Added and Clear Limitation, and Page's Device is Not a Single-Integrated Circuit</u>

Again, to summarize Applicants' representative's position on the limitation potential of language in the preamble of a claim, it has long been recognized by the Federal Courts that if the preamble of a claim is "necessary to give life, meaning, and a vitality" to the claim, then it should be construed as a claim limitation. See, e.g., *Kropa v. Robie*, 187 F. 2d 150, 152 (CCPA 1951). If, on the other hand, the preamble merely states the purpose or the

intended use of the invention, then the preamble cannot be said to constitute or explain a claim limitation and is of no significance to claim construction. See, e.g., *Pitney Bowes Inc. v. Hewlett-Packard Co.*, 182 F. 3d 1298, 1305 (Fed. Cir. 1999). Indeed, in section 2111.02 of the MPEP, the MPEP states that:

> [a]ny terminology in the preamble that limits the structure of the claimed invention must be treated as a claim invention. See e.g., *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F. 2d 1251, 1257, 9 USPQ 2d 1962, 1966 (Fed. Cir. 1989) (The determination of whether preamble recitations are structural limitations can be resolved only on review of the entirety of the application "to gain an understanding of what the inventors actually invented and intended to encompass by the claim.")

In other words, under current case law, there are no simple rules that can be applied to particular language in a preamble to determine whether or not the language represents a limitation, but, instead, <u>any</u> language that limits the structure of the claimed invention must be treated as a limitation. Again, in a claim that claims a "subsystem controller implemented as a single integrated circuit for control of a device or subsystem within an electronic system," the phrase "implemented as a single integrated circuit" most definitely and comparatively narrowly limits the structure of the claimed invention. In <u>The Electrical Engineering Handbook</u>, Dorf, Richard, CRC Press, 1993, page 614, an "integrated circuit" or "IC" is defined as: "an assembly of miniature electronic components simultaneously produced in batch processing, on or within a single substrate, which performs an electronic circuit function." In other words, an integrated circuit is what is commonly referred to a chip. The Page reference describes "a board-level system" (Page, page 1, sentence immediately preceding the first element of a bulleted list) that is further described in Page as a "small, 17 x 9 cm, printed circuit board which conforms to the Inmos TRAM standard" (Page, page 4, lines 2-3). A collection of discrete components soldered to, and electronically interconnected by, signal lines on a printed circuit board is not an integrated circuit. A board-level implementation of microprocessor/FPGA coprocessors employing discrete components soldered to PCB signal lines would unambiguously and definitely fall well outside the claim scope, as intended by Applicants. In view of current case law, Applicants' representative cannot understand how such language could possibly be considered not limiting. Please note that, as discussed above, the Examiner's assertion that the FPGA is a

single-IC subsystem controller is completely without basis. It is not. It is, instead, a co-processor included in a board-level system.

The Sudo Reference Does Not Disclose a Subsystem Controller

In a previous response, Applicants' representative characterized Sudo as follows:

> Sudo does not disclose a single-integrated-circuit implementation of a subsystem controller. Instead, in the figures referred to, and cited by, the Examiner, Sudo shows a standard collection of discrete components included within a computer system. As one example, the Examiner asserts that element 5A of the Figure 4 in Sudo teaches a controller programmed to display information. In fact, as noted in Sudo on lines 13-15, the box labeled 5A in Figure 4 is a liquid crystal display driver, or, in other words, a set of software routines that are run on the CPU to control the LCD 5. Element 5A of Figure 4 is not a controller programmed to display anything. Instead, it is a program. Sudo does not disclose a subsystem controller, because, as pointed out in the Background of the Invention section of the current application, a subsystem controller is a processing component independent of the CPU of the system, that, in part, functions to offload computing tasks from the central processing unit of the system (current application, page 1, lines 19-23). Sudo, by contrast, discloses a software control program that runs on the central processing unit of the system.

In response, the Examiner states, in section 22 of the Office Action, that "[h]owever, the LCD Driver (Element 5A of Figure 4) is a program which controls information displayed on the LCD. The CPU (Element 7 of Figure 4) is programmed with the LCD driver to control display information on an LCD display, as seen in Figures 8a-j. (Column 4, lines 13-24) Sudo has in fact disclosed a subsystem controller programmed to control display of information on an LCD display."

Applicants' representative hopes, in view of the above discussion of the meaning of the term "subsystem controller," that the Examiner can now clearly understand that a program running on the CPU of a computer system is not a subsystem controller. It is not a subsystem controller, as defined in the Specification, and it is not a subsystem controller by any definition of the term currently used and understood by computer-system designers. Subsystem controllers include processing components distinct from the main processors of a computer system, and are used to offload computing tasks from the main processors, and to decrease bus traffic within computer systems, as clearly stated in the Specification.

In summary, Applicants' representative believes that the 35 USC §102(b) rejection of claim 6 and the 35 USC § 103(a) of claim 1 are improper. On the basis of claim construction principles, the Examiner may not doubly employ the FPGA, included as a component in Page's board-level system, as both a single IC subsystem controller and as a subsystem controlled by the subsystem controller. Page's board-level system is not an integrated circuit, and is not a subsystem controller. The FPGA is not a subsystem controller, clearly not containing the list of components claimed as components of the subsystem controller claimed in claim 1. The Page reference is simply irrelevant to the invention clearly claimed in claims 1-10, and clearly described in the Specification.

Based on the above remarks, Applicants' representative respectfully requests reconsideration of the application in its early allowance.

Respectfully submitted,
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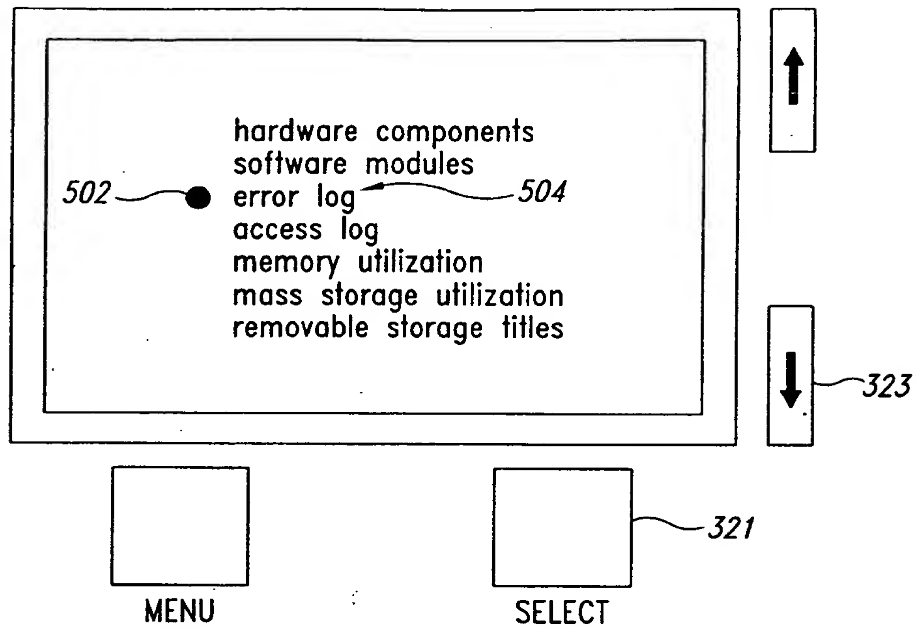
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software modules
error log
access log
memory utilization
mass storage utilization
removable storage titles
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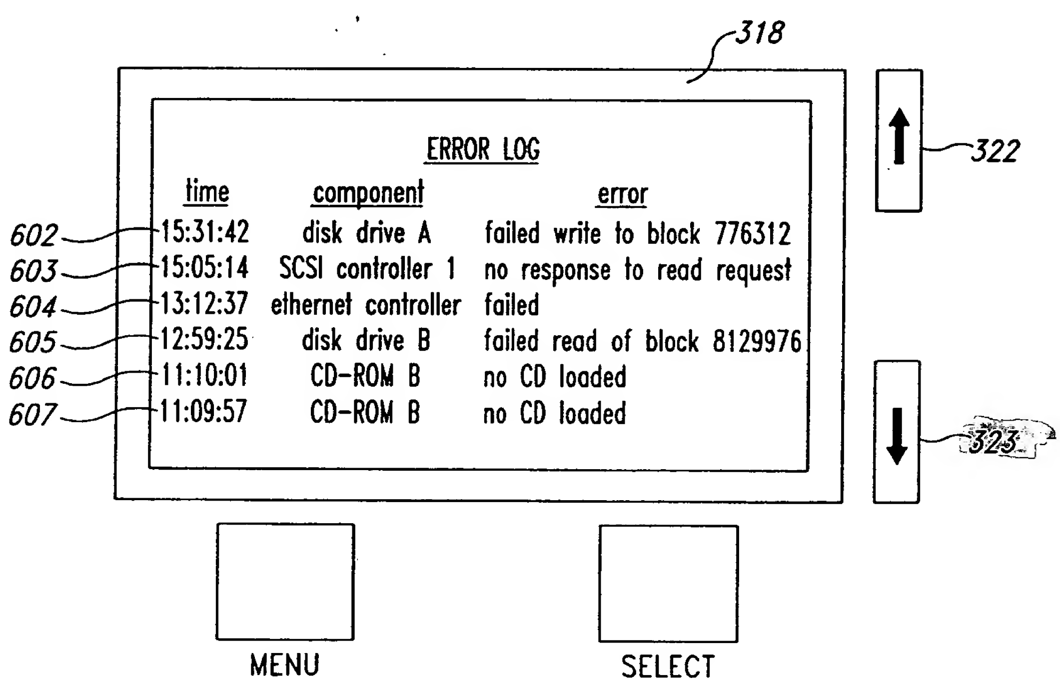
504
323
321
MENU
SELECT

Fig. 5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component
error
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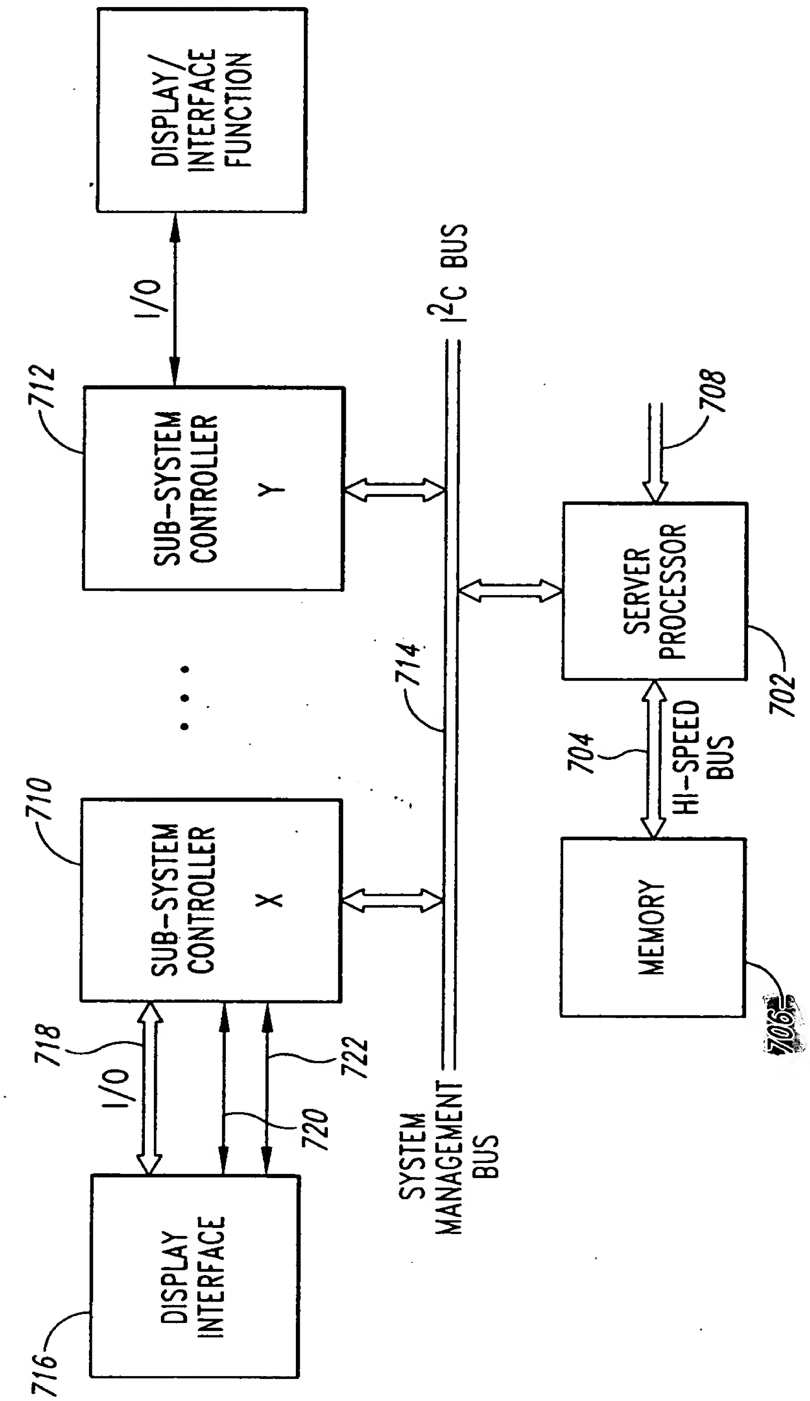
603 15:05:14 SCSI controller 1 no response to read request
604 13:12:37 ethernet controller failed
605 12:59:25 disk drive B failed read of block 8129976
606 11:10:01 CD-ROM B no CD loaded
607 11:09:57 CD-ROM B no CD loaded
322
323
MENU
SELECT

Fig. 6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INTERFACE
FUNCTION
I/O
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SUB-SYSTEM
CONTROLLER
Y
I^2C BUS
708
SERVER
PROCESSOR
702
714
704
HI-SPEED
BUS
710
SUB-SYSTEM
CONTROLLER
X
MEMORY
706
718
I/O
720
722
SYSTEM
MANAGEMENT
BUS
DISPLAY
INTERFACE
716

Fig. 7